WHAT IS CLAIMED IS:

1. A method of testing an integrated circuit comprising the steps of:

observing a selected parameter at a selected test node;

detecting an error at the selected test node in responses to said step of observing; and

stepping a current to the integrated circuit from a reference level by a selected current step representing the detected error.

2. The method of Claim 1 and further comprising the steps of:

observing a selected parameter at a second selected test node;

detecting a second error in response to said step of observing the selected parameter at the second selected test node; and

stepping the current to the integrated circuit by a second selected step representing the second error, the current being a sum of the selected step and the second selected current step and representing the error and the second error.

3. The method of Claim 1 and further comprising the steps of:

allowing the current to settle to an initial level after initiation of a test mode; and

stepping the current to the reference level from the initial level.

4. The method of Claim 3 wherein the selected parameter comprises a differential voltage.

5. The method of Claim 2 wherein the selected step and the second selected step are binary weighted current steps.

6. The method of Claim 1 and further comprising the step of initiating a test mode in response to power-up of the integrated circuit.

7. A method of testing an integrated circuit including a plurality of test nodes comprising the steps of:

initiating a test mode;

during a first time interval of the test mode, stepping a level of a supply current of the integrated circuit to a calibration level;

observing parameters at the plurality of test nodes to detect errors;

during a second time interval of the test mode, selectively stepping the level of the supply current in response to a number of errors detected; and

decoding the level of the supply current to identify the detected errors.

8. The method of Claim 7 wherein said step of stepping the level of the supply current comprises the substeps of:

representing an error at each test node with a binary weighted current; and

selectively summing the binary weighted currents proportionate to the number of errors detected to generate a corresponding step of the level of the supply current.

9. The method of Claim 7 wherein said step of initiating comprises the step of initiating the test mode at power-up of the integrated circuit.

10. The method of Claim 9 and further comprising the step of allowing an initial current to the integrated circuit to settle during a third interval prior to the first interval of the test mode.

11. The method of Claim 7 wherein the integrated circuit operates in response to an oscillator output signal and said method further comprises the step of counting a number of periods of the oscillator output signal during the first and second intervals of the test mode.

12. The method of Claim 7 wherein said step of observing the parameters at the plurality of test modes comprises the substeps of:

introducing an offset at an input to a chopper stabilized amplifier forming a part of the integrated circuit; and

observing an offset voltage an output of the integrated circuit.

13. The method of Claim 7 wherein said step of observing comprises the substep of measuring a differential voltage offset at a selected one of the test nodes.

14. The method of Claim 11 and further comprising the step of stepping down the level of the supply current at the end of second interval, said step of measuring time period timed by said step of stepping the level of the supply current to the calibration level and said step of stepping down the level of the supply current at the end of the second interval.

15. An integrated circuit comprising:

a plurality of functional blocks each associated with a test node for observing an associated operating parameter;

detecting circuitry for detecting errors at said test nodes during a test mode; and

a plurality of parallel current sources for selectively stepping a supply current to said integrated circuit in response to errors detected by said detecting circuitry during said test mode.

16. The integrated circuit of Claim 15 wherein said plurality of parallel current sources are sized to selectively step said supply current in binary weighted steps.

17. The integrated circuit of Claim 15 wherein said detecting circuitry comprises a difference amplifier for monitoring a differential voltage at a selected one said test nodes.

18. The integrated circuit of Claim 15 further comprising a current source for selectively stepping said current to a calibration level during said test mode.

19. The integrated circuit of Claim 15 further comprising circuitry for initiating said test mode.

20. The integrated circuit of Claim 19 wherein said circuitry for initiating said test mode comprises voltage level detection circuitry for initiating said test mode on power-up of said integrated circuit.